Concurrent Programming through the JTAG Interface for MAX Devices

February 1998, ver. 2 Product Information Bulletin 26

Introduction

In a high-volume printed circuit board (PCB) manufacturing environment, time-to-market is critical for designers. For this reason, Altera offers designers and manufacturing engineers programming options that minimize production time and increase throughput. One of these options is concurrent programming, which is the simultaneous programming of multiple complex programmable logic devices (CPLDs) that support in-system programmability (ISP). This product information bulletin compares concurrent programming to traditional CPLD programming (i.e., sequential programming), and discusses concurrent programming through the IEEE 1149.1 Joint Test Action Group (JTAG) interface for Altera® MAX® 9000 (including MAX 9000A), MAX 7000S, and MAX 7000A devices.

Concurrent Programming vs. Sequential Programming

Concurrent programming can decrease in-system programming time when programming a board with multiple ISP-capable CPLDs or with only a few CPLDs. The time required to program multiple ISP-capable CPLDs is slightly longer than the time required to program the largest device on a PCB. In contrast, sequential programming requires devices to be programmed one device at a time; thus, the sequential programming time is equal to the sum of the individual programming times for each CPLD.

Table 1 compares concurrent programming and sequential programming times for a PCB with 18 devices. With sequential programming, an additional 65 seconds is needed to program the PCB compared to concurrent programming. In a high-volume manufacturing environment, where thousands of boards may need to be programmed and tested, concurrent programming can substantially reduce the time needed to bring a product to market.

Table 1. Comparison of Concurrent Programming vs. Sequential Programming

Programming	Devices per Board	Programming Time per Device (Seconds)	Total Programming Time (Seconds)
Concurrent programming	18	4	7
Sequential programming	18	4	72

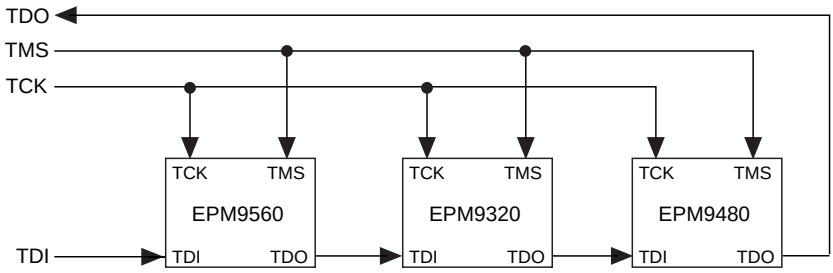
Programming through the IEEE 1149.1 (JTAG) Interface

Concurrent programming of ISP-capable CPLDs through the IEEE 1149.1 JTAG interface reduces the complexity of the manufacturing process. During production, implementing ISP through the JTAG interface allows all ISP-capable devices to be chained together in a JTAG chain, simplifying programming and testing. The JTAG chain can be extended to include non-ISP-capable JTAG devices for easier device testing. The time required to program the JTAG chain is slightly longer than the time required to program the largest device in the chain.

Concurrent Programming in Altera ISP-capable CPLDs

Altera ISP-capable CPLDs allow devices within the same family to be concurrently programmed, reducing programming times. Data is serially shifted into multiple devices along the JTAG chain, and then programming pulses are applied simultaneously to all the devices. Figure 1 illustrates concurrent programming through a JTAG chain of three Altera MAX 9000 devices.

Figure 1. Concurrent Programming of Three MAX 9000 Devices through an IEEE 1149.1 JTAG Chain



The time required to concurrently program multiple devices in a JTAG chain can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \sum_{\text{All Devices}} \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells for only the largest device
$Cycle_{PTCK}$ = Number of test clock (TCK) cycles to program each device
f_{TCK} = TCK frequency

Table 2 shows the concurrent programming times for 1, 2, 10, and 100 devices in a JTAG chain.

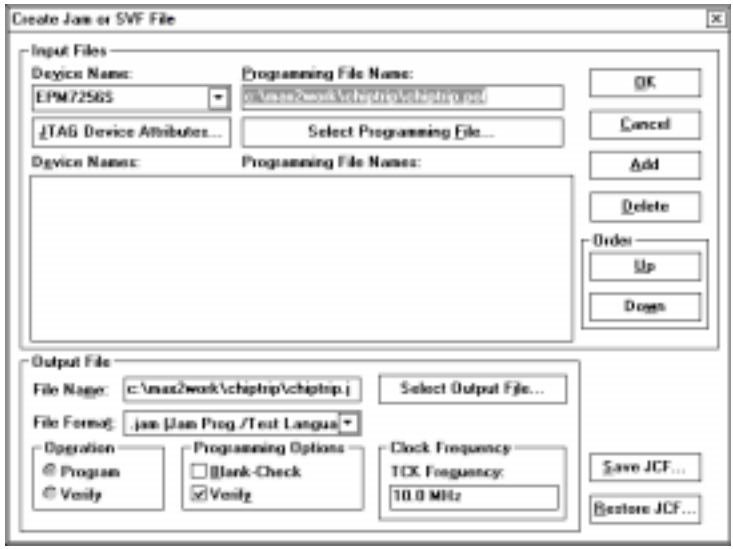
Table 2. Concurrent Programming Times

Family	Device	Programming Times (Seconds) *Note (1)*			
		1 Device	2 Devices	10 Devices	100 Devices
MAX 9000	EPM9560, EPM9560A	12.25	12.49	14.43	36.24
	EPM9480, EPM9480A	12.05	12.27	14.07	34.26
	EPM9400	11.85	12.06	13.70	32.24
	EPM9320, EPM9320A	11.65	11.84	13.34	30.21
MAX 7000S	EPM7256S	6.57	6.71	7.82	20.27
	EPM7192S	5.82	5.93	6.80	16.60
	EPM7160S	5.47	5.57	6.30	14.61
	EPM7128S	5.19	5.27	5.89	12.86
	EPM7064S	4.62	4.67	5.05	9.37
	EPM7032S	4.33	4.37	4.63	7.62
MAX 7000A, *Note (2)*	EPM71024A	3.07	3.19	4.13	14.78
	EPM7512A	3.01	3.07	3.54	8.88
	EPM7384A	3.00	3.04	3.40	7.41
	EPM7256A	6.57	6.71	7.82	20.27
	EPM7128A	5.19	5.27	5.89	12.86
	EPM7064A	2.96	2.97	3.02	3.65
	EPM7032A	2.95	2.96	2.99	3.30

Note:
(1) Times are provided for devices programmed at a TCK frequency of 10 MHz.
(2) Programming times for MAX 7000A devices are preliminary. For more information, contact Altera Applications at (800) 800-EPLD.

A Jam File (**.jam**) or Serial Vector Format (**.svf**) File can be used to concurrently program MAX 9000, MAX 7000S, or MAX 7000A devices. Both of these file formats use concurrent programming algorithms exclusively. An in-circuit tester or embedded processor shifts in data and perform concurrent programming. Designers using Altera devices and ISP benefit from this process on the manufacturing floor, because concurrently programming a device with in-circuit testers decreases the programming time, thereby decreasing the production time. You can use the **Create Jam or SVF File** dialog box in the MAX+PLUS® II software to create Jam or SVF Files. See Figure 2.

Figure 2. Create Jam or SVF File Dialog Box



For more information on using concurrent programming for Altera ISP-capable CPLDs, see *AN 39 (JTAG Boundary-Scan Testing in Altera Devices)* and *AN 85 (In-System Programming Times for MAX 9000 & MAX 7000S Devices)* in this handbook.